REMARKS

Applicants respectfully request reconsideration of the above-captioned application. New claims 4-6 have been added to round out the scope of protection being sought. Claims 1-6 are currently pending.

The Office Action of May 23, 2003 includes an objection to the drawings suggesting that reference number 310 is not described in the specification. Applicants respectfully point to page 3, line 16, where this reference number is used to refer to the etch regions such as shown in Figure 2 as well as Figures 4D and 4E. In light of this disclosure, Applicants respectfully request that the objections to the drawings be withdrawn.

The Office Action includes a rejection of claims 1-3 under 35 U.S.C. §102(e) as allegedly being anticipated by the *Lee* patent (U.S. Patent No. 6,245,635). This rejection is respectfully traversed.

The *Lee* patent concerns itself with a method of fabricating shallow trench isolation and is designed to prevent "dishing" of fill in the trenches, such as shown by the concave lines of Figure 1B. This dishing is caused during a polishing step for wide trenches wherein the polishing agents tend to erode the central portion more than the edge portions adjacent the polishing stop layers. The *Lee* patent, as shown in Figures 3A-3E etches trenches 308 into a substrate through a mask layer 304 and a pad oxide layer 302. Thereafter, a silicon oxide layer 316 is placed in the trenches and on top of the mask. Ion implantation 318 creates regions 322 of hardened material such that when a polishing step

takes place the dishing effect is less pronounced. Thereafter, the regions 322 and additional silicon oxide is removed to create the planar structure shown in Figure 4D.

In stark contrast to the *Lee* patent fabrication method, the present invention addresses a completely different problem using a completely different approach. Specifically, the present invention relates to a method of reducing notching due to over etching during a reactive ion etching (RIE) process. When RIE is performed and passed through a silicon layer on a sequentially-stacked structure of a silicon layer, an insulating layer and a silicon substrate, the lower portion of the silicon layer tends to be over etched with unnecessary lateral etching because the etching ions are reflected from the insulating layer due to an electrical potential that is formed thereon. The present invention minimizes the notching effect in a lower portion of the silicon layer when RIE is performed to pass through the silicon layer on a sequentially-stacked structure of silicon layer, and insulating layer and a silicon substrate by forming trenches in the insulating layer to expose the silicon substrate. In this way, when the silicon layer is formed on the insulating layer to fill the trenches, and a patterning of the silicon layer forms first etch regions, these etch regions can pass through the silicon layer to include the trenches. Because the trenches pass through the insulating layer, the reactive ions can be discharged through the substrate thus minimizing notching. The more closely aligned the edges of the trenches are to the etch regions, the less pronounced any residual notching is. This is illustrated by the SEM photographs of Figures 5 and 6 (prior art systems) compared to Figure 7 (the present invention).

Given the present invention and the *Lee* patent which addresses very different problems using different procedures to achieve distinct results, the rejection is apparently based on the idea that coincidentally the words of the claim happened to read on the prior art. Applicants respectfully disagree.

The Office identifies as the stack structure a silicon layer 316, an "insulation layer" 304 and a silicon substrate 300. The layer 304 is actually a mask layer and Applicants note the existence of the add oxide layer 302. The mask layer is used to form the trenches or recessed regions 310 in the substrate. Thereafter, a silicon oxide layer 316 fills the trenches. What is not shown, however, in the *Lee* patent is the recitation of claim 1 of patterning the silicon layer to form first etch regions, which pass through the silicon layer, to include the trenches. There is no such patterning step in the *Lee* patent. See Figure 4C and the description thereof, for instance. It is noted that after the polishing step, an etch step is performed to remove an upper level of the silicon oxide 316 and the polishing stop layer 322. However, this is not a patterning step and does not pass through the silicon layer to include the trenches. In fact, it is evident that the trenches remain completely filled.

Hence, Applicants respectfully submit that the *Lee* patent does not anticipate the present invention.

With respect to claim 2, it is also noted that the *Lee* patent does not disclose patterning the silicon layer positioned between trenches to form second etch regions which are narrower than the first etch regions. This is illustrated in Figures 4D and 4E by etch region 304. Because the etch regions are narrower, it is unnecessary for a trench to be

formed in the insulating layer. The *Lee* patent does not show this aspect of the present invention.

Finally, as noted previously, with respect to claim 3, the *Lee* patent does not show removing the silicon filled in the trenches to expose the silicon substrate.

New claims 4-6 include the distinguishing recitations of claims 1-3, but also further capture the concept that the trenches in the insulating layer expose the top surface of the silicon substrate, rather than forming trenches therein as in the *Lee* patent.

In light of the foregoing, Applicants respectfully request reconsideration and allowance of the above captioned application. Should any residual issues exist, the Examiner is invited to contact the undersigned at the number listed below.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

Date: August 19, 2003

By: _____
Charles F. Wieland III
Registration No. 33,096

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620